2SK3018

Small switching (30V, 0.1A)

- **Features**

Low on-resistance.
Fast switching speed.
Low voltage drive (2.5V) makes this device ideal for portable equipment.
Easily designed drive circuits.
Easy to parallel.

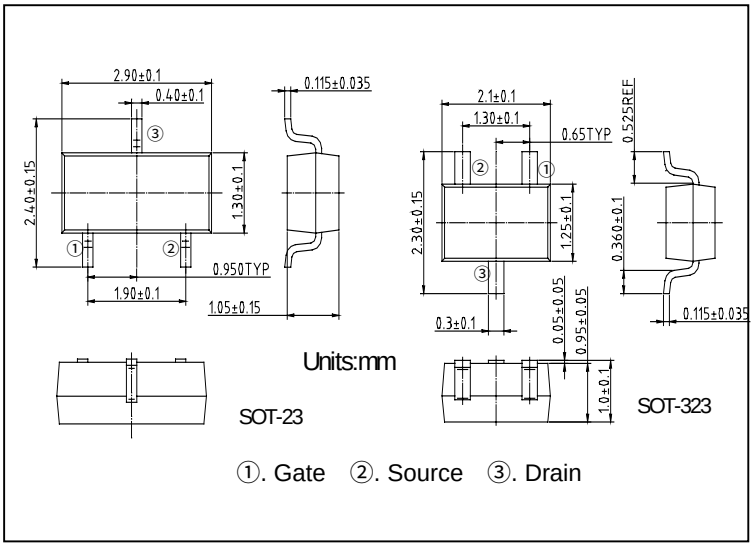
- **Applications**

Interfacing, switching (30V, 100mA)

- **Structure**

Silicon N-channel MOSFET

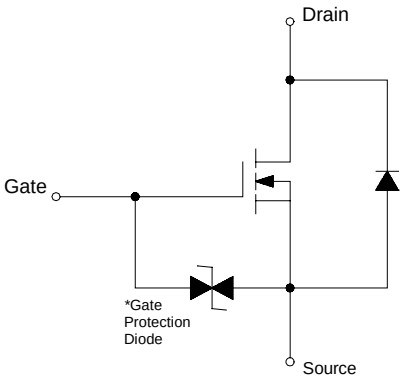
• External dimensions



- **Absolute Maximum Ratings (Ta = 25°C)**

Parameter		Symbol	Ratings	Units
Drain-source voltage		V_{DSS}	30	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	Continuous	I_D	100	mA
	Pulsed	I_{DP}	200	mA
Reverse drain current	Continuous	I_{DR}	100	mA
	Pulsed	I_{DRP}	200	mA
Total power dissipation		P_D	200	mW
Channel temperature		Tch	150	°C
Storage temperature		Tstg	-55~+150	°C

- **Equivalent circuit**



- **Electrical Characteristics (Ta = 25°C)**

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Gate-source leakage	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	----	----	±1	μA
Drain-source breakdown voltage	$V_{(BR)DSS}$	I_D=10μA,V_{GS}=0V	30	----	----	V
Zero gate voltage drain current	I_{DSS}	V_{DS}=30V,V_{GS}=0V	----	----	1	μA
Gate threshold Voltage	$V_{GS(th)}$	V_{DS}=3V,I_D=100μA	0.8	----	1.5	V
Static drain-source on-state resistance	$R_{DS(ON)}$	I_D=10mA,V_{GS}= 4V	----	5	8	Ω
	$R_{DS(ON)}$	I_D=1mA,V_{GS}=2.5V	----	7	13	Ω
Forward transfer admittance	Yfs	V_{DS}=3V,I_D=10mA	20	----	----	mS
Input capacitance	Ciss	V_{DS}=5V V_{GS}=0V F=1 MHz	----	13	----	pF
Output capacitance	Coss		----	9	----	pF
Reverse transfer capacitance	Crss		----	4	----	pF

Turn-on delay time	td(on)	I_D=10 mA ,V_{DO}=5V V_{GS}= 5V R_L=500Ω R_{GS}=10Ω	----	15	----	ns
Rise time	tr		----	35	----	ns
Turn-off delay time	td(off)		----	80	----	ns
Fall time	tr		----	80	----	ns

- **Typical Performance Characteristics**

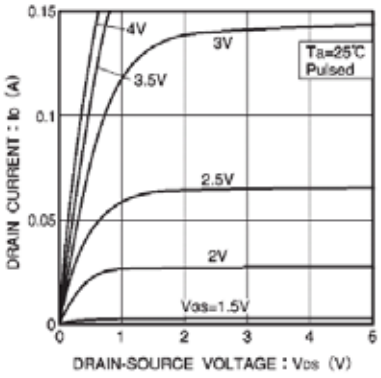


Fig.1 Typical output characteristics

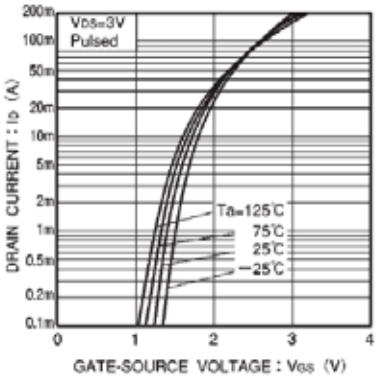


Fig.2 Typical transfer characteristics

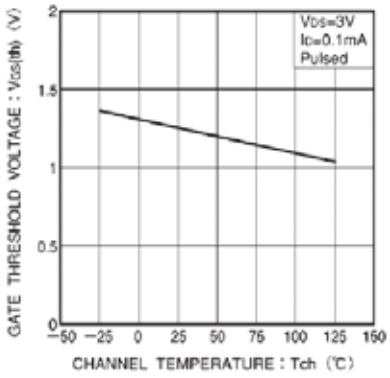


Fig.3 Gate threshold voltage vs. channel temperature

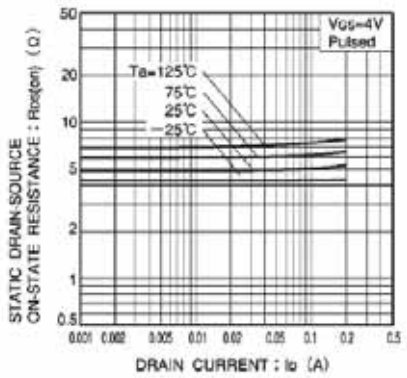


Fig.4 Static drain-source on-state resistance vs. drain current (Ⅰ)

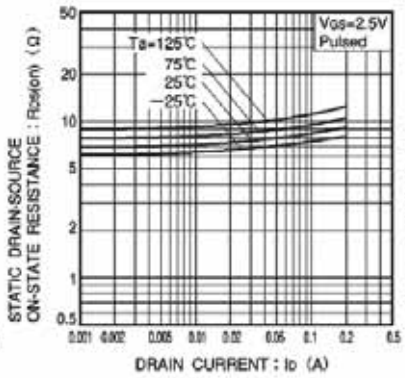


Fig.5 Static drain-source on-state resistance vs. drain current (Ⅱ)

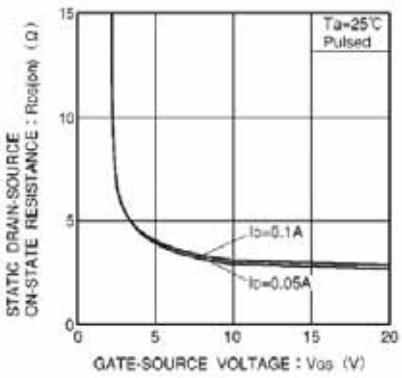


Fig.6 Static drain-source on-state resistance vs. gate-source voltage

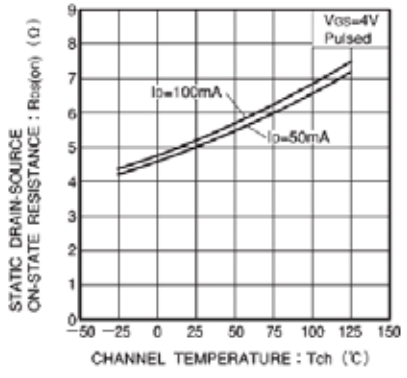


Fig.7 Static drain-source on-state resistance vs. channel temperature

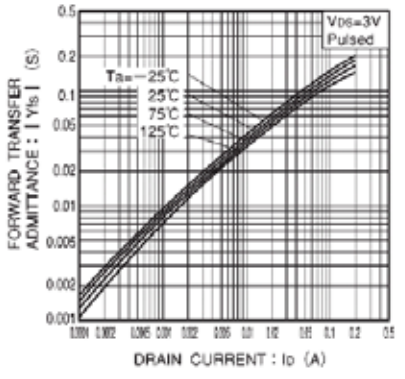


Fig.8 Forward transfer admittance vs. drain current

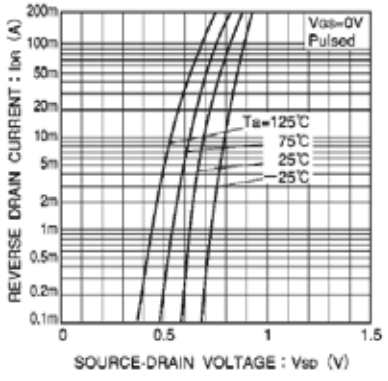


Fig.9 Reverse drain current vs. source-drain voltage (Ⅰ)